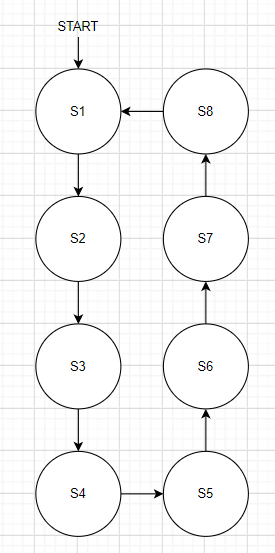
**Project 3**

**Problem 1.**

1. Design a finite state machine (FSM) with at least 7 states. You decide the inputs and outputs. Draw the state diagram of your FSM. Make sure that your design be different from those used by other students. If your design is identical to some design used by other students, further investigation will be conducted and you will be asked to revise your design and redo the work.

Diagram Website

[https://app.diagrams.net/#G10J3Gjh1Z2gQxG-U2IW0d\_qpRBVJfF5Wl](https://app.diagrams.net/%23G10J3Gjh1Z2gQxG-U2IW0d_qpRBVJfF5Wl)



1. Model A: model your FSM with SV using the regular case statements with binary state coding.
2. Model B: model your FSM with SV using the regular case statements with one-hot state coding.
3. Model C: model your FSM with SV using the reversed case statements with one-hot state coding.
4. Write one testbench to verify all the models.
5. Synthesize all the models and filling the table below.

|  |  |  |  |
| --- | --- | --- | --- |
|  | Model A | Model B | Model C |
| Number of total cells | 16 | 63 | 28 |
| Total cell area | 5256 | 20430 | 11880 |
| Power Consumption | 1.5956nW | 2.4610mW | 2.0346mW |

Table. Comparisons of FSMs

**Problem 2.** Design a 4-bit Gray code adder.

1. The adder has three components: two 4-bit Gray-to-binary converters, a 4-bit binary adder, and a 5-bit binary-to-Gray code convertor.
2. Write a synthesizable SV code.
3. Synthesize the design (Choose osu05\_stdcells.db as your target library, generate the netlist file in Verilog)
4. Find the gate counts, the area, and the power of the synthesized circuit using the DC report command.
   1. **Gates: 16 cells, 24 nets, 13 ports.**
   2. **Cell Area: 6480.**
   3. **Power: 4.9461 mW for dynamic power**
   4. See report for more details
5. By simulation, compare the SV model and the synthesized Verilog netlist with the same testbench. **Simulated both. Appears identical?**

**Problem 3.**

For Problem 1 of your project 2, you have an SV behavioral model for your S1.

1. Synthesize the model.
2. Find the gate counts, the area, and the power of the synthesized circuit using the DC report command.
   1. **Gates: 16 cells**
   2. **Cell Area: 7740.**
   3. **Power: 3.1881 mW total power**
3. By simulation, compare the SV model and the synthesized Verilog netlist with the same testbench. Simulated Both, appears identical.